REMARKS

Claims 1-18 and 20 are pending in the application. Claims 1, 9, 10, and 18 have been amended. No new matter has been added. Reconsideration is respectfully requested in view of the amendments to the claims and the following remarks.

I. Allowable Subject Matter

Applicant wishes to thank the Examiner for allowing claim 20.

II. The §102 Rejections

Claims 1-18 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,721,884 ("Pereira").

Claim 1, as amended, recites a method for dynamically programming a field programmable gate array (FPGA) in a coprocessor. In particular, the method includes providing a processor and a coprocessor that is separate from the processor in that the coprocessor is coupled to the processor through a bus that is external to the processor. The coprocessor includes a field programmable gate array (FPGA)that is dynamically programmed to perform a function responsive to a determination that the field programmable gate array (FPGA) is not programmed to perform the function.

A. Pereira Fails to Disclose a Coprocessor Coupled to a Processor Through a Bus That is External to the Processor In Which the Coprocessor Includes a Field Programmable Gate Array (FPGA)

As shown in FIG. 1, Pereira discloses a pipelined processor including a configurable functional unit 18 that is capable of executing reconfigurable instructions. The configurable functional unit 18 can be reconfigured at run-time (see Abstract; col. 5, ll. 38-60). Pereira,

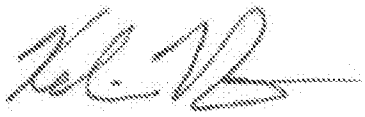
however, fails to disclose providing a coprocessor that is separate from a processor in that the coprocessor is coupled to the processor through a bus that is external to the processor, in which the coprocessor includes a field programmable gate array (FPGA), as recited in claim 1. Instead, Pereira discloses a processor that includes a configurable functional unit 18 that is *internal* to the processor. The ALU functional unit 16 and the configurable functional unit 18 are both internal to the processor. Consequently, Pereira fails to disclose a coprocessor coupled to the processor through a bus that is external to the processor, in which the coprocessor includes a field programmable gate array (FPGA). Applicant respectfully submits that claim 1 is, therefore, allowable over Pereira.

Claims 2-8 depend from claim 1, and are allowable for at least the reasons that apply to claim 1.

Independent claims 9, 10, 18 and 20 (and the claims that depend therefrom) incorporate limitations similar to claim 1, and are also allowable for at least the reasons that apply to claim 1.

Applicant submits that claims 1-18 and 20 are allowable over the reference cited above, and are in condition for allowance. Should any unresolved issues remain, the Examiner is invited to call the undersigned at the telephone number indicated below.

Respectfully submitted,
SAWYER LAW GROUP LLP



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